Identifying and eliminating Digital Light Processing™ failure modes through accelerated stress testing

Abstract: Reliability is a critical aspect of any commercial or consumer product. The challenge of developing reliable high technology products in a rapid-paced, highly competitive marketplace is discussed. Specific examples of accelerated stress tests applied to the Digital Micromirror Device™ (DMD™) and other Digital Light Processing™ (DLP™) components are reviewed.

Delivering reliable products is always a challenge. Further constraints on product development include low cost, rapid time-to-market and limited samples for evaluation. To meet these challenges, innovative and aggressive reliability development techniques must be implemented. The approach implemented by Texas Instruments Digital Imaging program is referred to as “accelerated stress testing” or AST.

Although this is not a new concept, many people are unfamiliar with it. Similar techniques are known as accelerated life testing, highly accelerated life testing (HALT™), step stress testing, reliability growth testing, and test, analyze and fix (TAAF), among others. Each of these reliability development techniques has the common goal to find potential failure modes as rapidly as possible providing opportunities to eliminate the failure mode prior to product delivery.

This article describes the Digital Imaging reliability development approach, provides examples of stress testing and summarizes the reliability of Digital Light Processing (DLP) products.

Introduction
DLP-based products consist of six major components including a light source, optics, color filters, a Digital Micromirror Device (DMD), electronics and a projection lens, as illustrated in Figure 1. The DMD consists of an array of micromirrors. Each micromirror is 16 microns square on a 17-micron pitch. Figure 2 provides an exploded view of a micromirror. Micromirrors are individually addressable and rotate ± 10 degrees when an electrostatic field attracts the micromirror toward the underlying address electrode. Detailed information about DMD fabrication and operation is provided in reference 1.

Accelerated stress testing approach
In its simplest form the accelerated stress testing (AST) approach implemented by Digital Imaging consists of five (5) steps:

1) Identify potential product weaknesses
2) Increase test stresses in order to force weaknesses to failure
3) Investigate the root cause of the failure
4) Implement appropriate corrective actions

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5) Repeat items two through four for each weakness until it is no longer cost-effective to implement additional corrective actions

At this point, the inherent design weakness of the product is usually well beyond the product’s operating limits.

The following paragraphs describe some of the stress tests used to improve, verify and demonstrate DMD reliability. The sections following the discussion about DMD reliability address the AST approach to other levels of DLP electromechanical subassemblies.

Identifying and accelerating potential DMD failure modes
The first application of accelerated stress testing by Digital Imaging occurred with the DMD. In 1992, when the DMD was still under development, little was known about DMD reliability. The reliability department organized an informal failure mode and effect analysis (FMEA) by bringing together a group of DMD experts. Since the DMD materials and processes were (and still are) similar to other semiconductor devices, the group was joined by semiconductor experts from throughout Texas Instruments. These experts brainstormed possible ways a DMD could fail, identifying several dozen potential failure modes that included:

- Hinge fatigue (mirrors wearing out due to metal fatigue in the hinges)
- Mirrors breaking (due to handling, shock and vibration)
- Hinge memory (mirrors becoming nonfunctional due to metal creep)
- Nonfunctional mirrors (mirrors that stick or otherwise fail due to billions of landings)

For each failure mode identified during the FMEA, a test was designed to measure its potential risk. The tests varied in duration, ranging from hours to several years before confirming results would be available. There was not enough time to use normal operating stress levels, resulting in waits ranging from months to years for results. The program also needed to produce rapid results to help establish priorities for the emerging Digital Imaging business, including answering whether the DMD was reliable. If it was not reliable, what were the reasons? Could design and/or process changes improve device reliability? For these reasons it was imperative to apply acceleration factors to several tests. Accelerated stress testing contributed essential information to address these important issues.

Rapid mirror switching—hinge fatigue
One of the most critical failure modes identified during the FMEA review was the possibility of mirrors breaking due to hinge fatigue as a result of the hinges twisting and bending. Normal operation in a DLP application switches the micromirrors once every 200 to 300 microseconds. To achieve a five-year lifetime (assuming only 1000 operating hours per year), the micromirrors would need to switch over $90 \times 10^9$ times. No known microelectromechanical system (MEMS) had ever achieved such lifetimes.

To address this concern a simple accelerated stress test was designed. The test cycled DMD micromirrors on and off every 20 microseconds, accelerating this failure mode by a factor of 10. Within several weeks the test had already surpassed $90 \times 10^9$ cycles and eventually reached 1 trillion cycles without failure.

More recently, this test was repeated. The devices again surpassed 1 trillion cycles and continued beyond 1.7 trillion cycles without failure. This test has demonstrated at least 10 years of normal use in any application and over 50 years in most applica-
tions. Interestingly, the devices on this test have accumulated over $2 \times 10^{18}$ (two quintillion) mirror cycles and are still on test with no evidence of hinge fatigue!

The results of this accelerated stress test were critical to our understanding of DMD reliability. Although a failure was not identified nor accelerated, the test was able to quickly demonstrate that hinge fatigue was not a concern for reliable device operation. This allowed Digital Imaging to focus on other priorities and concerns.

**Shock and vibration—handling and package integrity**

Considering the microscopic size of the micromirrors, the FMEA questioned if mirrors could easily break during assembly, handling or use in a DLP product. To address this concern a sequence of mechanical tests was extracted from the Texas Instruments Semiconductor Qualification Procedure. The test consisted of mechanical shock (1500g, 0.5 millisecond pulses), vibration (20g peak, 20 to 2000 hertz), and acceleration (10,000g centrifugal force).

With the exception of some early package integrity failures and an occasional loose particle inside the device package, all micromirrors were undamaged and unaffected by this series of testing. To further investigate the mechanical integrity of the DMD, a mechanical shock test was designed to increment shock levels to the point of failure. Shock levels of 1500g, 3000g, and 5000g resulted in no damage to the micromirrors or the package. At 10,000g, package damage was evident and the test was stopped. Similar robust performance was confirmed through repeated vibration and acceleration testing.

This series of accelerated stress tests demonstrated that the micromirrors were mechanically robust. The package damage occurred at stress levels well above the design requirement. A particle reduction program addressed random loose particles in the package. This sequence of stress tests provided rapid feedback to the DMD process engineers resulting in a dramatic reduction of particles.

**High temperature operation—hinge memory and nonfunctional (stuck) mirrors**

During early development testing it was observed that devices failed more rapidly at high temperatures. This was noted as a potential failure mode during the FMEA. DMDs were characterized at various temperatures ranging from 0°C to +85°C and nonfunctional micromirrors were strongly correlated with high operating temperature. The root cause of the failures was attributed to metal creep in the hinge material and was referred to as “hinge memory.” For example, a micromirror continually addressed toward the offside (that is, when the micromirror appears dark in a projected image) will exhibit a small amount of residual tilt toward the offside when all electrostatic fields are removed. The micromirror will continue to operate properly until the residual tilt accumulates and exceeds approximately 35 to 40% of the 10-degree rotation angle. At this point, the micromirror will only rotate to the offside and appear as a dark pixel on a projected image.3, 2

Once the correlation was found between hinge memory and high temperature, accelerated stress tests were designed to take advantage of this knowledge. A life test at high temperature and high duty cycle (the micromirrors always addressed toward one side) forced DMDs to fail within a few hours. This allowed rapid evaluation of a series of new materials and processes. Within several months tests identified hinge materials exhibiting less metal creep and therefore longer lifetimes due to hinge memory. Additional testing helped develop improved material processes and a more effective way to dynamically control the micromirrors. In a relatively short development period, hinge memory lifetime increased dramatically, exceeding 100,000 hours.

**DMD reliability demonstration**

References 2, 3, and 4 provide more detail on the failure modes discussed above as well as other DMD failure mechanisms. Accelerated stress tests greatly increased our learning cycles by shortening the time required to realize experimental results. We also were able to make rapid decisions about proposed design and process changes. Consequently, the DMD entered the commercial marketplace with great expectations for high reliability. To date over 100,000 DLP systems are in use throughout the world and the DMD is proving to be even more reliable than expected. Recent calculations demonstrated a DMD mean time between failures (MTBF) of over 119,000 hours. Life tests, as discussed in reference 2, have demonstrated lifetimes exceeding 100,000 hours under normal operating conditions.

**Application of accelerated stress testing to DLP systems**

The success of AST on DMD reliability lead to its application on other DLP assemblies. Early testing on
prototype DLP engines indicated very promising product reliability.5 The following sections describe examples of follow-on stress testing activities as well as lessons-learned on a variety of products.

Mechanical shock
One of the first stress tests applied to a DLP product was mechanical shock. There was concern that the critical alignment of DLP components (light source, optics, color filter, DMD, electronics and projection lens) would degrade during assembly, handling and use.

To simulate severe handling and stimulate any mechanical weaknesses, a series of mechanical shocks (illustrated in Figure 3) were applied to the original VGA (640x480-resolution) design. The tests started with pulses of 5G, 11 milliseconds in all six axes and progressed to 25G, 11 milliseconds with no failures or indications of degraded operation. At 30G the test caused a glass color wheel filter to chip. (This DLP projector with one DMD used a spinning color wheel with red, green, and blue filters to create sequential color.) Further investigation found the color wheel assembly improperly supported and free to move when excited in the Y-axis.

Shortly after the investigation started, customers reported a small number of their products exhibited chipped color wheel filters upon receipt of the DLP engine. Apparently, the units were being subjected to mechanical forces equivalent to 30G, 11 milliseconds in the shipping process. Fortunately, Digital Imaging engineers had already identified the source of failure through AST and had corrective actions nearly implemented. The support structure of the color wheel assembly was improved and the shipping containers redesigned to provide better protection. Customer failures attributed to chipped color wheels were eliminated and overall mechanical robustness of the product was enhanced.

To obtain fundamental information about DLP mechanical integrity, mechanical shock AST was continued with a goal of reaching 50G. The testing identified additional weaknesses resulting in further design modifications. The testing continued through 50G, 8 milliseconds with no failures or degradation. This series of testing was stopped when it eventually achieved 105G, 5 milliseconds in all six axes. The product remained fully functional through 105G although the zoom lens was slightly deformed. The test was ceased due to the limitations of the mechanical shock table being used.

Several essential lessons-learned from mechanical shock AST include:
• Earlier testing would have highlighted weaknesses prior to shipping products
• Test results correlated well with reported customer failures
• Using AST, rapid feedback was provided to the Digital Imaging design team resulting in rapid corrective action and closure
• AST-based mechanical shock improved the mechanical integrity of follow-on DLP products and designs

Power cycling
Another early example of stress testing DLP systems was the application of rapid power cycling. Early prototype systems were placed on life tests to simulate actual operation. This test consisted of a power cycle (the system was automatically turned off, then on again) once every three hours. A computer controlled the power cycling and also recorded failure codes when a system failed to turn on. A review of life test data indicated that there were some intermittent failures but no trends were apparent. There were so few power cycle attempts that no statistically significant conclusions could be drawn.

To learn more about possible power cycling failures the life test was redefined and modified. Its new purpose was to stimulate failure modes, not simulate possible operating scenarios. Instead of a power cycle once every three hours (eight times per day), the new

Figure 3. DLP engine on an electrodynamic vibration table for mechanical shock testing.
life test performed a power cycle once every minute. Within the first day, the test accumulated 1440 power cycle attempts on each system under test. The data clearly showed that there was one failure for every thirteen power-on attempts. In addition, the data was statistically significant and demonstrated numerous causes of failure originating from firmware errors, power supplies, lamps, miscellaneous electronics, and test equipment.

With this detailed information available, the Digital Imaging design team was able to assign detailed actions and systematically eliminate the root cause of each failure. The rate of failure was rapidly reduced to one intermittent failure for each 800 attempts and eventually reached the point where the tests consistently accumulated thousands of power cycles with no failures.

The lessons learned from the previously discussed mechanical shock AST are also applicable to the power cycling stress testing. By stimulating and eliminating failure modes, production failures can be minimized, customer failures avoided, and learning cycles increased, resulting in a more reliable product available to the market sooner. In this example and subsequent development efforts, power cycling AST has resulted in DLP products with more robust electrical designs.

Temperature stress testing
A very common stress test uses temperature as an acceleration factor. Digital Imaging used a modified version of the typical temperature-based life test to more rapidly accelerate and identify product weaknesses. Temperature stress testing is performed at the engine, subsystem or assembly level during the development process to identify and eliminate design weaknesses. It is performed in three steps.

Step 1—High temperature step stress
The test sample is operated in a temperature chamber where it is subjected to increasing ambient temperatures until failure is observed. Dwell and transition times are modified based on time estimates needed to reach thermal stability and the capabilities of the temperature chamber. A typical test scenario is:

- Operate the unit in a temperature chamber at +40°C (maximum specified operating temperature) for two hours allowing the chamber and unit under test to achieve thermal equilibrium
- Perform an operational test (acceptance test) at the end of the thermal soak

An application of temperature stress testing
Temperature AST was recently applied to a new DLP product in the large-venue product line. A projector engine with XGA (1024x768) resolution included three DMDs to achieve superior brightness and image quality. The engine development program employed temperature stress testing during system development to verify and gain confidence in system performance over temperature. The development effort was for a drop-in replacement of the 500W 3-DMD SVGA (800X600) engine with XGA (1024X768) resolution. The 500W engine consisted of a base plate, lamp power supply, 3-DMD light tube assembly and flex cables connecting the DMDs to the formatter memory and control boards, image processor, signal converter and motherboard. **Figure 4** shows an engine ready to be tested in a temperature chamber. Temperature stress testing was performed on a sample of one unit. The observations are listed in **Table I.**
The results of these tests showed that the design had very good margin with regard to system temperature specifications. All anomalies occurred outside of the +10°C to +40°C specification limits. Noise on the image was observed while operating the unit at +65°C. These results formed the basis for a design change necessary to increase noise margin on a phase locked loop (PLL) clock circuit. The high temperature step stress test was discontinued after a lamp power supply failure occurred at +75°C, which is 35°C above the upper system operating temperature limit of +40°C. The low temperature step stress test resulted in no failures until a lamp power supply would not stay energized at –50°C, 60°C below the lower operating specification of +10°C! A single failure was observed in the second cycle of extreme temperature cycling from -40°C to +50°C due to a lamp power supply shut down. The lamp power supply was replaced and an additional 6 temperature cycles were completed without failure. A second unit completed an additional 24 temperature cycles from -40°C to +50°C with no failures. The testing also verified successful operation of thermal protective devices shutting down the system in case of overheating.

Following completion of temperature stress testing, the engine passed a rigorous image quality evaluation, requiring only minor adjustments to converge the three DMDs. While a DLP product will not encounter these temperature extremes in real life applications, the results provide a high degree of confidence that the system will work under the more benign conditions expected in the actual use environment.

**Voltage stress tests**

Voltage stress testing is a method used to determine a design’s tolerance to fluctuations in power supply voltages. The testing employed by Digital Imaging consisted of:

- Verification that the unit under test met performance requirements under any combination of power supply voltages (within specification limits)
- Testing to determine operational limits of critical supply voltages (beyond specification limits)

For the first test, a matrix of system-level power supply voltages could be compiled to evaluate each

<table>
<thead>
<tr>
<th>Test</th>
<th>Temp.</th>
<th>Finding</th>
<th>Resolution</th>
</tr>
</thead>
<tbody>
<tr>
<td>High temperature step stress</td>
<td>+55°C</td>
<td>Lamp power supply shut off</td>
<td>Verified protection circuit function. Disabled to continue test</td>
</tr>
<tr>
<td>High temperature step stress</td>
<td>+65°C</td>
<td>Noise on image</td>
<td>Changed design to improve filtering on formatter PLL clock circuit</td>
</tr>
<tr>
<td>High temperature step stress</td>
<td>+70°C</td>
<td>Parked mirrors</td>
<td>Verified protection circuit function. Disabled to continue test</td>
</tr>
<tr>
<td>High temperature step stress</td>
<td>+75°C</td>
<td>Lamp power supply shut off</td>
<td>Showed good margin to +40°C specification limit – discontinued test</td>
</tr>
<tr>
<td>Low temperature step stress</td>
<td>-10°C</td>
<td>Parked mirrors</td>
<td>Verified protection circuit function. Disabled to continue test</td>
</tr>
<tr>
<td>Low temperature step stress</td>
<td>-50°C</td>
<td>Lamp power supply shut off</td>
<td>Showed good margin to +10°C specification limit – discontinued test</td>
</tr>
<tr>
<td>Extreme temperature cycling</td>
<td>+50°C</td>
<td>Lamp power supply shut off</td>
<td>Survived numerous temperature cycles</td>
</tr>
</tbody>
</table>

Figure 4. Large-venue XGA 500W engine installed in temperature chamber for temperature testing.
combination of minimum and maximum voltage tolerances. A test would then be performed for each combination of voltages. If the unit under test had only a few supply voltages (i.e., +3.3 VDC, +5 VDC and +12 VDC), testing every combination of limits could be done with $2^3$ settings of the supply voltages as in Table II.

Table II. Matrix to test every combination of high and low specification values on three power supply voltages.

<table>
<thead>
<tr>
<th>Test run</th>
<th>+3.3 VDC</th>
<th>+5.0 VDC</th>
<th>+12 VDC</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>± 5%</td>
<td>± 5%</td>
<td>± 10%</td>
</tr>
<tr>
<td>1</td>
<td>+3.135</td>
<td>+4.75</td>
<td>+10.8</td>
</tr>
<tr>
<td>2</td>
<td>+3.135</td>
<td>+4.75</td>
<td>+13.2</td>
</tr>
<tr>
<td>3</td>
<td>+3.135</td>
<td>+5.25</td>
<td>+10.8</td>
</tr>
<tr>
<td>4</td>
<td>+3.135</td>
<td>+5.25</td>
<td>+13.2</td>
</tr>
<tr>
<td>5</td>
<td>+3.465</td>
<td>+4.75</td>
<td>+10.8</td>
</tr>
<tr>
<td>6</td>
<td>+3.465</td>
<td>+4.75</td>
<td>+13.2</td>
</tr>
<tr>
<td>7</td>
<td>+3.465</td>
<td>+5.25</td>
<td>+10.8</td>
</tr>
<tr>
<td>8</td>
<td>+3.465</td>
<td>+5.25</td>
<td>+13.2</td>
</tr>
</tbody>
</table>

Systems or subsystems that are more complex may use a large number of supply voltages. Verification of full system performance should also include performance over a variety of temperature conditions. Exhaustive testing of every combination of voltage and temperature would require a significantly large number of tests. If the system had five DC supply voltages, testing every combination requires $2^5$ or 32 settings of supply voltages. Performing these tests at room, hot and cold temperature would increase the total number of tests to 96. If exhaustive testing were too time-consuming, the concept of orthogonal arrays may be used to reduce the number of tests. For example, if a system had five supply voltages, operation over the supply voltage tolerances may be verified with only 16 settings using a half-factorial orthogonal array as in Table III.

Testing within the specified voltage tolerance range of the system power supply is inadequate to ensure performance when production variation is introduced. To address this, voltage stress testing beyond specification tolerances may be applied. One method is to increase and decrease a single supply voltage until failure occurs while other supply voltages are held constant (usually at nominal values). When a failure is observed, the design team analyzes the cause of failure and either implements corrective actions to increase margin or concludes that adequate margin has been demonstrated to meet performance requirements. Voltage stress tests are often repeated over temperature or combined with accelerated temperature stress testing to further enhance the reliability of the system.

Timing margin improvements realized through accelerated stress testing

Voltage stress testing was applied during the 3-DMD
XGA development program to accelerate failure mechanisms early in the design process. The 3-DMD XGA electronics use five DC supply voltages: +5 VDC and +3.3 VDC for digital logic, ±5 VDC for analog video signal processing and +12 VDC for cooling fans and DMD reset voltage generation. A half-factorial orthogonal array was selected to investigate the effects and interactions of voltage tolerances.

The array summarized in Table III includes combinations of high and low specification limits on DC power supply voltages. The system passed acceptance tests performed for each combination of supply voltage settings in Table III and passed at low and high system temperature specifications (+10°C and +40°C). However, the design team was not satisfied with just performance to specification, and applied AST methods to discover the limits of the design. Each supply voltage was individually varied while the others were held constant.

System performance was continuously monitored as in Figure 5. During one such test of the +3.3 VDC digital logic supply voltage operating at +40°C, a noise pattern was observed on the image with the +3.3 VDC slightly below specification at +3.1 V. While this is below the system specified minimum voltage of +3.2 VDC, the design team concluded that it did not provide adequate margin for production variation. An analysis of the problem found that a timing parameter was being violated at these conditions. The formatter assembly was modified to provide additional timing margin. This simple modification significantly improved margin on the +3.3 VDC supply voltage while providing confidence the system will tolerate power supply variation in production.

**Conclusion**

The use of stress testing beyond specification levels provides significantly more information than just whether a design passes or fails. By testing designs to the point of failure, Digital Imaging can better understand how systems fail and implement designs that are more robust. In addition, once failure modes are identified through stress testing, designs can be readily evaluated by using the stress test to accelerate the known failure mode.

This article provided several examples of how AST was applied to DMDs and DLP technology. There are numerous other AST examples addressing other failure modes. Using AST, DMD reliability has been improved dramatically. DMD lifetimes are estimated at over 100,000 operating hours and over 1.7 trillion mirror cycles. The successful implementation of AST on DMD development lead to a similar approach on other DLP systems with equally successful results.

Several important findings and conclusions from the DLP accelerated stress testing program include:

- Development testing needs to *stimulate* failures not *simulate* use
- Early testing is capable of highlighting design weaknesses prior to shipping products
- Testing correlates well with customer failures
- Using AST, rapid feedback was provided to the Digital Imaging design engineers resulting in faster corrective action implementation
- AST deployment has improved mechanical integrity, thermal robustness, electrical performance stability and overall reliability of DLP products.

**Trademarks**

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References


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