Supporting Information

for Adv. Mater., DOI: 10.1002/adma.201104889

Carbon-Carbon Contacts for Robust Nanoelectromechanical Switches

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Supporting Information: Carbon-carbon contacts for robust nanoelectromechanical switches

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Keywords: diamond-like carbon, nanoscale devices, nanoelectromechanical systems
**Supporting Information:**

*S.1 Device Fabrication and Imaging*

**Figure S1.** Schematic of process flow for fabrication of freestanding carbon-carbon NEM switches. The process is amenable to construction of both cantilevered and suspended CNT architectures with a variety of electrode materials.

Devices were fabricated on silicon substrates passivated with a 200-nm silicon nitride film (Supporting Figure S1A). A continuous, nitrogen-doped DLC film 140 nm in thickness was next deposited on the wafers. A tetrahedral amorphous form of DLC (ta-C) was used with a measured resistivity of ~50 Ω·cm. The composition of this DLC film was characterized by Raman spectroscopy and found to be predominantly amorphous diamond ($sp^3$-hybridized carbon, see Figure S2 and Methods Section S.2). A 70-nm aluminum thin film (10-nm titanium adhesion layer) patterned by photolithography and liftoff was then used as an etch mask to define the electrode structures in the DLC film. The exposed DLC was etched through to the silicon nitride by reactive ion etching (RIE) using CF$_4$ (3 sccm) and O$_2$.
(100 sccm) gases at a pressure and power of 30 mTorr and 400 W, respectively. The aluminum etch mask was then stripped by RIE using BCl₃ (10 sccm), Cl₂ (15 sccm) and He (140 sccm) gases at a pressure and power of 10 mTorr and 75 W respectively (Figure S1B). 

Platinum traces and wire bonding pads (100-nm Pt, 10-nm Cr adhesion layer) were defined over the DLC electrodes using photolithography and liftoff (Figure S1C). A conformal silicon dioxide sacrificial/dielectric layer was then deposited by PECVD using SiH₄ (16 sccm), Ar (24 sccm), and N₂O (32 sccm) gases at a pressure of 9.7 mTorr, substrate temperature of 400 C, and power of 498 W (Figure S1D). The thickness of this layer ultimately defines the gap between the CNT and electrode in the completed devices. Via holes were then opened in the oxide film to allow continuity between the metal CNT contacts and wire bonding pads (Figure S1E). These vias were first defined by photolithography then etched through to the Pt using 6:1 buffered oxide etch (BOE, CAUTION: BOE contains hydrofluoric acid which is extremely hazardous).
Figure S2. Raman spectra of DLC electrodes. (A) Characteristic Raman spectrum of a DLC electrode. Also shown is the background signal taken from a region in which the underlying silicon nitride-coated silicon substrate was exposed (see Figure S1). Inset is an optical micrograph with green dots showing the points on the underlying silicon nitride-coated silicon substrate and DLC from which the background and DLC electrode spectra were collected respectively. Scale bar is 5 µm. (B) Spectrum of the DLC electrode (same as in (A)) after baseline correction. (C) Gauss-Lorentz fit to the DLC Raman spectrum in (B). All spectra were collected using a 532 nm laser. See Methods Section S.2 for details.

The samples were cleaned in O₂ plasma (22 sccm) for 3 minutes at 160 mTorr pressure and 40 W power to ensure a hydrophilic surface for uniform and repeatable CNT dispersion, as well as strong adhesion between the electron-beam resist and the substrate in subsequent steps. Arc-discharge grown multi-walled CNTs (n-Tec, Norway) were suspended in 1,2-dichlorobenzene by sonication and serially diluted to a concentration of ~0.07 mg/mL. The CNT solution was then dispersed over the samples by placing a droplet in the center of the chip and allowing it to roll back and forth across the surface approximately 25 times. The sample was then blown dry with nitrogen (Figure S1F).

Electron beam lithography and liftoff were used to define metal contacts to the CNTs (Figure S1G). The samples were spincoated with hexamethyldisilazane as an adhesion promoter, immediately followed by ZEP-520 electron beam resist, and then baked on a hot plate for 3 minutes at 150 C. The samples were exposed on a Raith 150 EBL/SEM system to define contacts between the CNTs and vias to the underlying platinum traces. A palladium film 75 nm in thickness was then sputtered and lifted off in Anisole. The two-point resistance of the palladium-contacted CNTs (which includes the contact resistance) was measured to be
on the order of 100 kΩ, which is consistent with other reports \cite{1-3}. To complete the devices, CNT structures were released by etching away the exposed silicon dioxide in 10:1 BOE. After etching in BOE, the samples were rinsed in two consecutive DI water baths, then in isopropanol. Special care was taken not to allow the surface of the sample to dry when transferring between the BOE, deionized water, and isopropanol to prevent surface CNT-substrate adhesion. The samples were then dried in a critical point dryer (Leica) to complete the devices (Figure S1H). Finally, devices were imaged using an FEI Nova NanoSEM in immersion mode to confirm that the CNTs were properly freestanding above the DLC electrodes and to measure characteristic dimensions.
S.2 Raman Spectroscopy

Figure S3. Raman spectroscopy of cantilevered and suspended CNTs. (A-D) Characterization of cantilevered CNTs. (A) Optical micrograph showing palladium contact to a CNT which is cantilevered over a gold electrode. Scale bar is 5 µm. Note that devices with gold electrodes were constructed specifically for Raman spectroscopy analysis as the background signal from the DLC electrodes and underlying silicon nitride was too great to resolve the contribution from individual CNTs. (B) Scanning electron micrograph showing the actual CNT in (A). Scale bar is 500 nm. Substrate is tilted 52° about the horizontal axis of the image. (C) Raman spectroscopic map of the region shown in (A). Intensity is proportional to the integrated area of the G peak region. Scale bar is 500 nm. (D) Representative spectrum taken from the map in (C). Dashed black lines show Gauss-Lorentz fits to the D, G, D’, and G’ bands. Solid black line is the sum of the fits. (E-H) Characterization of suspended CNTs. (E) Optical micrograph showing palladium contacts with a CNT suspended between them over a gold electrode. Scale bar is 5 µm. (F) Scanning electron micrograph showing the actual CNT in (E). Scale bar is 1 µm. Substrate is tilted 45° about the horizontal axis of the image. (G) Raman spectroscopic map of the region shown in (E). Intensity is proportional to the integrated area of the G peak region. Scale bar is 500 nm. (H) Representative spectrum taken from the map in (G). Dashed black lines show Gauss-Lorentz fits to the D, G, D’, and G’ bands. Solid black line is the sum of the fits.

Raman spectroscopy was performed using a Nikon Eclipse Ti-U inverted microscope outfitted with a Horiba Jobin Yvon LabRAM HR scanning confocal Raman spectroscopy system and an Andor Newton EMCCD. A 532 nm laser was used with a Nikon 100x CFI Plan Achromat objective.

Spectra collected from the DLC electrodes (Figure S2) were indicative of a predominantly sp²-hybridized carbon composition (approximately 80%). In particular, the
two peaks below 1300 cm$^{-1}$ were shown to weaken significantly at lower $sp^3$ contents [4]. In addition, the peak around 1750 cm$^{-1}$ disappears entirely with lower $sp^3$ content [4].

For spectroscopy of individual cantilevered and suspended CNTs (Figure 2E-F and Figure 3D-E), the Raman spectra were mapped in the device region with a step size of 0.15 µm and integration time of 1 second (see Figure S3). Initially it was difficult to isolate a signal from the CNTs themselves due to the large, broad-spectrum background signal from the underlying DLC electrodes and silicon nitride. Thus to enable more specific Raman analysis of the CNTs themselves, devices were also fabricated with gold electrodes (Figure 2E and Figure 3D) rather than DLC in addition to the devices with DLC used for electromechanical characterization. This provided a minimal background signal and clear identification of the CNT spectrum as shown in Figure 2E and Figure 3D. Given that the fabrication process flow was nearly identical, it is assumed that the defect density in these devices with gold electrodes is representative of that in the DLC devices. After mapping (Figure S3C), the individual spectra were fit using a Gauss-Lorentz fit to the D, G, D’, and G’ bands. The dashed lines in Figure S3D show the individual band fits, while the solid black line shows the sum of these bands, which closely matches the raw data.
Figure S4. Measurement of cycled on/off current from Figure 2D. (A) Segment of the input voltage train used for cycle testing. The input was alternately stepped between \( V_{HI} \) and \( V_{LO} \) (see (B)). Every 1,000 cycles, the input was held at \( V_{READ} = 22 \text{ V} \) (\( V_{PO} < V_{READ} < V_{PI} \)) between successive low and high steps to allow measurement of ‘off’ and ‘on’ currents (sampled at the blue and red points respectively) for a total of 1,000,000 cycles. Measured currents are shown in Figure 2D. (B) Current-voltage response for the cantilevered device shown in Figure 2A (same as that shown in Figure 2B) with \( V_{LO} \), \( V_{READ} \), and \( V_{HI} \) marked (see (A)). (C,D) Scanning electron micrographs of the carbon-carbon NEM switch in Figure 2D before and after the 1,000,000 cycles respectively. Scale bars are 250 nm. The substrate is tilted 52° about the horizontal axis of each image. The length of the CNT is the same in the two images to within the resolution of the image. There is a slight apparent increase in the diameter of the CNT in (D) relative to (C) which is attributed to the deposition of amorphous carbon during the SEM imaging performed after the cycling.

A Keithley 4200-SCS semiconductor characterization system (5 mV, 1 pA resolution) was used to characterize device current-voltage response (see for example Figure 2B and Figure 3B), as well as for cycle testing (Figure 2D, Figure S4, and Figure 3B) and logic gate characterization (Figure 4 and Figure S6). In all measurements, a 1 GΩ resistor was used in series (\( R \) in Figure 1A and Figure 4C). Measurements were conducted under vacuum (~10⁻⁶ Torr) within the chamber of a scanning electron microscope (FEI Nova NanoSEM). Pull-in and pull-out voltages were determined from the point in the measured current-voltage response at which there was a sharp increase or decrease in current respectively (see for example Figure S5).
Figure S5. Measured pull-in and pull-out voltages from Figure 3B. Pull-in and pull-out voltages were measured from the current-voltage plots in Figure 3B. The one-sided error bars are a result of the discrete steps in applied voltage (0.1 V steps) used to characterize the current-voltage responses shown in Figure 3. Given that, for example, pull-in would occur at some point within a 0.1 V step, we say that the true pull-in voltage is somewhere within one step (0.1 V) below the point at which a jump in current was observed. Similarly for pull-out, we assume that the true pull-out occurs somewhere within one step (0.1 V) above the point at which the sharp drop in current is first observed.

During characterization of the logic gates, the electrical potential of the pair of CNTs ($V_O$), computed based upon the measured current ($i_A + i_B$) through the resistor (1 GΩ), was taken as the output ($V_O = V_{BIAS} - (i_A + i_B)R$, see Figure S6). Here, two channels of the Keithley system were used to apply the two independent inputs $V_A$ and $V_B$, and measure the corresponding currents, $i_A$ and $i_B$. 
Figure S6. Construction of logic gates from pair of carbon-carbon NEM switches. (A) Schematic of the pair of cantilevered devices as they were used for logic operations. The inputs to the two CNTs are tied together and biased through a resistor, while their DLC electrodes are independently addressable. The output is taken as the electrical potential of the CNTs, \( V_o \), and is computed based upon the measured current flows, i.e. \( V_o = V_{\text{BIAS}} - (i_A + i_B)R \). (B) Optical micrograph showing the layout of multiple CNT NEM switches. Scale bar is 10 \( \mu \text{m} \). The inputs to all the CNTs in the devices are tied together as shown in (A), while their DLC electrodes are independently addressable. The inputs to the two cantilevered NEM switches used for the logic gates shown in Figure 4 are labeled \( V_A \) and \( V_B \). (C-F) Scanning electron micrographs (false color) of the CNT NEM switches shown in (B). Specifically, the switches shown in (C) and (F) were used for the logic operations described in Figure 4. All scale bars are 500 nm. Substrate is tilted 52° about the horizontal axis of the image in (C-F).

S.4 Device Response Time

To characterize the device response time (Figure 2C and Figure 3C), a step input \( V_{\text{IN}} \) = 8 V was applied to the device (Figure S7A) using a function generator (Agilent 33250A).

When the switch closes and current flows through the device, the electrical potential of the device electrode changes due to the potential drop across the series resistor. Thus the electrical potential of the electrode was taken as the device output and monitored using an oscilloscope (LeCroy 9348L). The second channel of the oscilloscope was used monitor the signal being input to the device from the function generator. This served as a reference signal against which to measure the delay in the device response (see details below).

Due to the small current levels (~10^{-9} A), the low input impedance of the oscilloscope (1 M\( \Omega \)) relative to the larger resistor (1 G\( \Omega \)) would result in a voltage response below the noise floor of the measurement if the oscilloscope were connected directly to the electrode (effectively shorting the resistor). A voltage follower constructed from an operational amplifier (Texas Instruments OPA541) was thus used as a buffer (10^{12} \Omega input impedance)
such that oscilloscope would not influence the potential of the electrode (Figure S7A). This buffer was found to have a highly repeatable delay of 4 ± 1 ns (Figure S7F-G). For simplicity, the time scale of the device output signal was shifted back 4 ns relative to the input signal to compensate for this delay in the plots shown in Figure 2C and Figure 3C. The original raw data is shown in Figure S7B-E.

In general, the required pull-in voltage of the devices was larger than the 8 V pulse from the function generator. To compensate, a negative offset bias ($V_{\text{offset}} < 0$) was also applied to the electrode of the device (Figure S7A) such that the total bias across the device itself was the difference of the input pulse and the offset bias, namely: $V_{\text{device}} = V_{\text{IN}} - V_{\text{offset}}$. The switch will thus close when $V_{\text{device}} \geq V_{\text{PI}}$. For the cantilevered device (Figure 2C), $V_{\text{PI}} = 23.4$ V. Accordingly, an offset of $V_{\text{offset}} = -15.5$ V was used such that $V_{\text{device}} = 8 + 15.5 = 23.5$ V (i.e., just above $V_{\text{PI}}$) when the input pulse reaches 8 V. For the suspended device (Figure 3C), $V_{\text{PI}} = 41.2$ V. An offset of $V_{\text{offset}} = -33.3$ V was thus used such that $V_{\text{device}} = 8 + 33.3 = 41.3$ V (again just above $V_{\text{PI}}$) when the input pulse reaches 8 V. For simplicity, $V_{\text{device}}$ is referred to as the “Input Voltage” in the plots in Figure 2C and Figure 3C. Similarly, the “Output Voltage” in Figure 2C and Figure 3C is equivalent to the difference of the switch output from the buffer and the offset voltage, namely: $V_{\text{switch output}} - V_{\text{offset}}$. In this way the plotted “output voltage” in Figure 2C and Figure 3C represents the change in potential across the series resistor due to current flow through the device.

As mentioned, the second channel of the oscilloscope was used to simultaneously monitor the signal input to the device from the function generator. This was used as a reference against which to measure the delay in the device response. However, if this reference signal were taken directly from the function generator to the oscilloscope, then the measured delay would be influenced significantly by parasitic capacitances/inductances arising in the external cables, etc. Thus to obtain a reference signal that was more indicative of the true input to the device, the step input from the function generator was also applied to a
continuous metal trace on the device chip (as done by Kaul, et al.\textsuperscript{[5]}) and monitored simultaneously using the oscilloscope. By using a reference signal which travels through the same external cables and similar trace lengths on the chip itself (and thus experiences the same resultant delays), we assume that delays due to parasitic losses exterior to the switch itself do not significantly affect the measurement.

Finally, we define the response time as the delay between the point at which the reference input signal reaches 8 V (where $V_{\text{device}} \approx V_{\text{PI}}$ and pull-in should initiate) and the time at which there is measurable output from the device, less the known delay in the operational amplifier-based buffer circuit (a highly repeatable 4 ± 1 ns, see above and Figure S7G). Given the total delay time of 14 ± 1 ns for the cantilevered device (Figure S7C) and the known op amp delay, this leads to a cantilevered device response time of 14 – 4 = 10 ± 2 ns. Similarly for the suspended device, the total delay time of 16 ± 1 ns (Figure S7E) leads to a suspended device time of 16 – 4 = 12 ± 2 ns when compensating for the buffer delay.
Figure S7. Characterization of device time response. (A) Schematic of the circuit used to characterize device response time. (B,C) Raw measured data ($10^9$ samples/sec) of the reference input and switch output for the cantilevered carbon-carbon NEM switch device shown in Figure 2A. These data have not been compensated for the buffer delay as was done in Figure 2C. There is a delay of $14 \pm 1$ ns between the point at which the reference input reaches pull-in level and when the buffer (switch) output begins to rise. Note that the output rises according to the slew rate of the operational amplifier. Due to the relatively low currents (below the specified bias current of the device), the observed slew rate and gain were somewhat lower than that specified by the manufacturer. (D,E) Raw measured data ($10^9$ samples/sec) of the reference input and switch output for the suspended carbon-carbon NEM switch device shown in Figure 3A. These data have not been compensated for the buffer delay as was done in Figure 3C. There is a delay of $16 \pm 1$ ns between the point at which the reference input reaches pull-in level and when the buffer (device) output begins to rise. Again note that the output rises according to the slew rate of the operational amplifier. Due to the relatively low currents (below the specified bias current of the device), the observed slew rate and gain were somewhat lower than that specified by the manufacturer. (F) Schematic of the circuit used for characterization of the intrinsic buffer circuit delay. The buffer delay is defined as the difference in time between the point at which the reference input pulse begins to rise and the point at which the buffer output begins to rise in response to this step input. (G) Input (reference) to the buffer circuit and measured output. There is a well-defined delay between the point at which the input begins to rise and the point at which the output begins to rise of $4 \pm 1$ ns. Subtracting this intrinsic buffer delay from the delay observed in (C) gives a cantilevered device response time of $14 - 4 = 10 \pm 2$ ns. Similarly, this gives a device response time of $16 - 4 = 12 \pm 1$ ns for the suspended device in (E).
Figure S8. Modeling device time response. A device having the geometry of the cantilevered NEM switch shown in Figure 2A (CNT length of ~500 nm, CNT diameter 24 nm, CNT-electrode gap of 115 nm) was simulated using a previously reported dynamic multiphysics model [6]. At \( t = 0 \) ns, a step input equal to \( V_{PI} \) is applied. (A) A CNT comprised of 30 concentric shells (i.e., a multi-walled CNT) is simulated. The assumption of 30 shells is based upon incrementally varying the number of shells in the simulation until the pull-in voltage matched with the experimentally-measured pull-in voltage (see Figure 2B). This is also consistent with the average number of shells reported for multi-walled CNTs obtained from the same source [7]. The plot shows the gap between the tip of the CNT and the electrode as a function of time, as well as the current through the device in response to the step input. The CNT makes contact with the electrode after approximately 6.6 ns, which serves as a lower bound on the response time of the device shown in Figure 2A. Inset shows the state of the device at the point of contact (6.6 ns). (B) Results of the simulation repeated for a CNT having the same geometry in (A) but only three concentric shells. The response time approaches one nanosecond.
Figure S9. Surface roughness of DLC electrodes. Image shows an atomic force microscopy topographic image of the surface of a DLC electrode obtained using a Park Systems XE-120 AFM in contact mode. The RMS roughness is 5 Å. Scale bar is 250 nm, height scale is 2 nm.

S.6 Demonstrating Logic Operations

As an example of the functionality of the carbon-carbon NEM switches, diode-resistor-type logic gates\textsuperscript{[8]} were constructed from a pair of cantilevered NEM switches (Figure 4A,B). The two CNTs were tied together electrically while the DLC electrodes associated with each switch were independently addressable and taken as the inputs (Figure 4C, see also Supporting Figure S6). The electrical potential of the pair of CNTs ($V_O$), computed based upon the measured current through the resistor, is taken as the output.

Figure 4D-G shows the various device states as they correspond to the outputs $V_O$ in Figure 4H,I as labeled. AND gates were constructed by applying a fixed bias ($V_{\text{BIAS}} = 40$ V) to the CNTs through a pull-down resistor $R$ (1 GΩ) and using the potential of the two electrodes as the inputs (Figure 4H). OR gates were constructed by grounding the CNTs ($V_{\text{BIAS}} = \text{GND}$) through a pull-up resistor $R$ and again using the electrode potentials as the inputs (Figure 4I). For the OR gate, a somewhat larger pulse was required to induce both CNTs to pull-in together to achieve state (D). The on-off ratio of the OR gate (state (G) to state (F)) was approximately 1500. The AND gate exhibited a lower on-off ratio (state (F) to...
state (G)) of 1.5, as it is largely limited by the high CNT-electrode contact resistance which prevents the CNT potential from being pulled fully down to ground when making contact with a grounded DLC electrode. As such, the reliable switching afforded by the carbon-carbon contact allows for demonstrations of functionality such as these logic gates. Future advances to various multi-electrode device architectures\cite{9-10} will enable complete, ultra-compact logic families using far fewer elements than common CMOS-based logic. These switches however will likely see more widespread application in hybrid NEM-CMOS devices as a means to reduce the rapidly growing power consumption of CMOS technologies will allowing for continued scaling of the silicon processes.\cite{11-13}

References